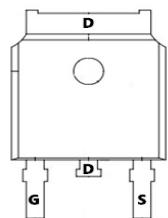


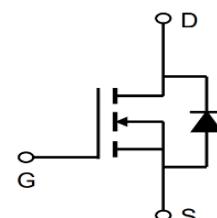
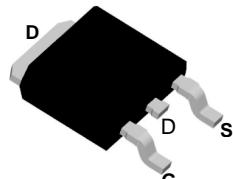
TM50N06AD

N-Channel Enhancement Mosfet

General Description <ul style="list-style-type: none"> Low $R_{DS(ON)}$ RoHS and Halogen-Free Compliant Applications <ul style="list-style-type: none"> Load switch PWM 	General Features <p>$V_{DS} = 60V$ $I_D = 48A$</p> <p>$R_{DS(ON)} = 13\text{ m}\Omega$ (typ.) @ $V_{GS} = 10V$</p> <p>100% UIS Tested 100% R_g Tested</p> 
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D:TO-252-3 L



Marking: 50N06A

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	60	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	A
		$T_C = 100^\circ C$	A
I_{DM}	Pulsed Drain Current ^{note1}	178	A
EAS	Single Pulsed Avalanche Energy ^{note2}	280	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.76	$^\circ C/W$
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TM50N06AD
N-Channel Enhancement Mosfet
Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=250\mu\text{A}$	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$\text{V}_{\text{DS}}=60\text{V}, \text{V}_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$\text{V}_{\text{GS}}=\pm20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	$\text{V}_{\text{GS(th)}}$	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\mu\text{A}$	1	2	3	V
Drain-Source On-State Resistance	$\text{R}_{\text{DS(ON)}}$	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_D=30\text{A}$	-	13	18	$\text{m}\Omega$
Forward Transconductance	g_{FS}	$\text{V}_{\text{DS}}=5\text{V}, \text{I}_D=30\text{A}$	30	-	-	S
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C_{iss}	$\text{V}_{\text{DS}}=25\text{V}, \text{V}_{\text{GS}}=0\text{V},$ $F=1.0\text{MHz}$	-	1698	-	PF
Output Capacitance	C_{oss}		-	185	-	PF
Reverse Transfer Capacitance	C_{rss}		-	80	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	$t_{\text{d(on)}}$	$\text{V}_{\text{DD}}=30\text{V}, \text{I}_D=2\text{A}, \text{R}_L=1\Omega$ $\text{V}_{\text{GS}}=10\text{V}, \text{R}_{\text{GEN}}=3\Omega$	-	12	-	nS
Turn-on Rise Time	t_r		-	5.2	-	nS
Turn-Off Delay Time	$t_{\text{d(off)}}$		-	38	-	nS
Turn-Off Fall Time	t_f		-	27	-	nS
Total Gate Charge	Q_g	$\text{V}_{\text{DS}}=30\text{V}, \text{I}_D=30\text{A},$ $\text{V}_{\text{GS}}=10\text{V}$	-	36	-	nC
Gate-Source Charge	Q_{gs}		-	9.9	-	nC
Gate-Drain Charge	Q_{gd}		-	6.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V_{SD}	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_S=30\text{A}$	-	-	1.2	V
Diode Forward Current <small>(Note 2)</small>	I_S		-	-	48	A
Reverse Recovery Time	t_{rr}	$\text{TJ} = 25^\circ\text{C}, \text{IF} = 30\text{A}$ $d\text{i}/dt = 100\text{A}/\mu\text{s}$ <small>(Note 3)</small>	-	35		nS
Reverse Recovery Charge	Q_{rr}		-	47		nC
Forward Turn-On Time	t_{ton}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $\text{Tj}=25^\circ\text{C}, \text{V}_{\text{DD}}=30\text{V}, \text{V}_{\text{G}}=10\text{V}, \text{L}=0.5\text{mH}, \text{Rg}=25\Omega$

Typical Performance Characteristics

Figure 1: Output Characteristics

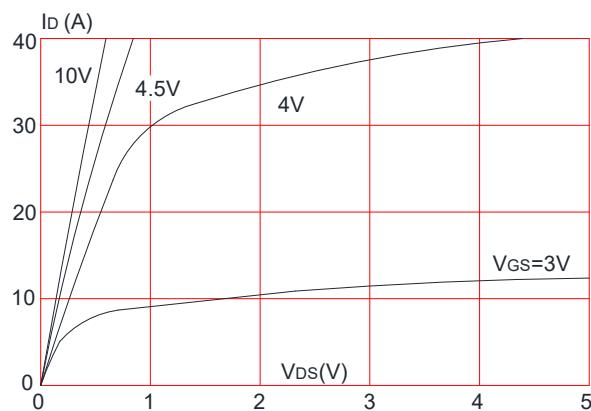


Figure 3: On-resistance vs. Drain Current

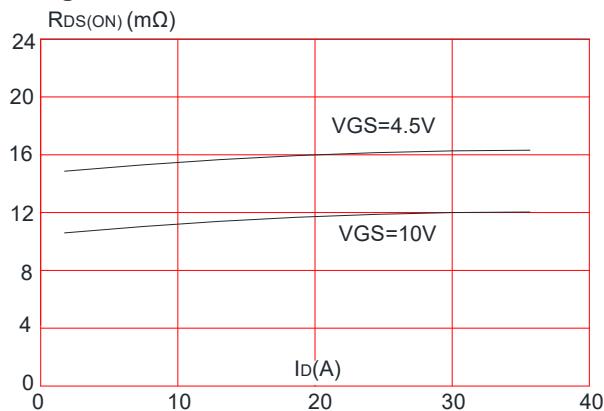


Figure 5: Gate Charge Characteristics

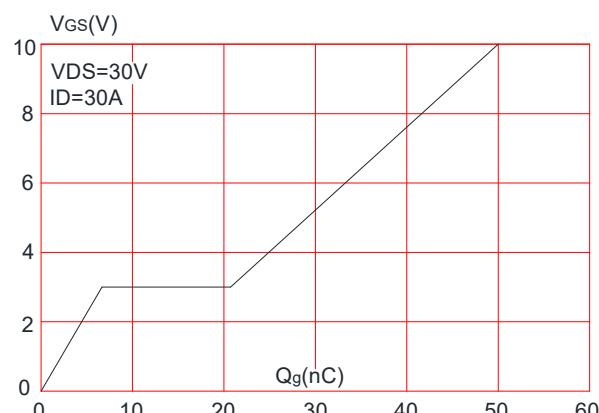


Figure 2: Typical Transfer Characteristics

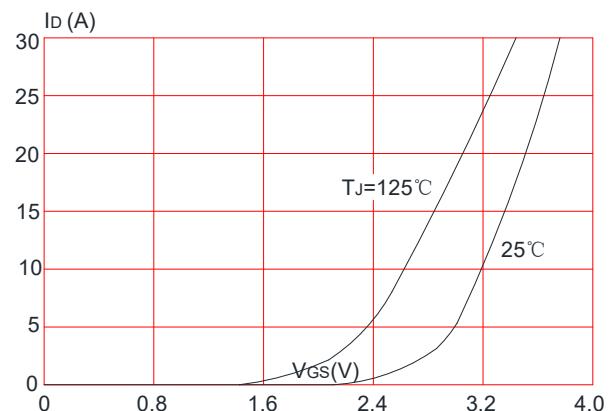


Figure 4: Body Diode Characteristics

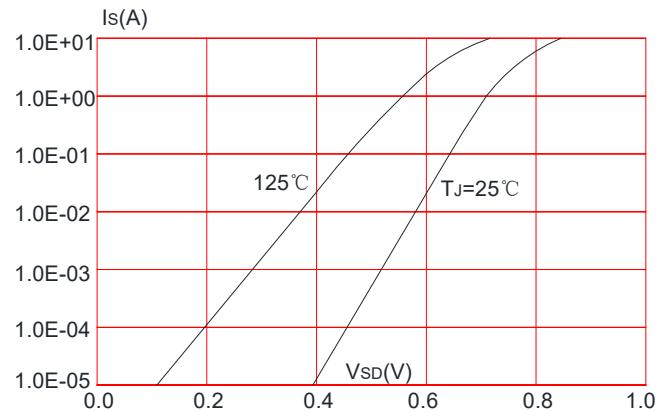


Figure 6: Capacitance Characteristics

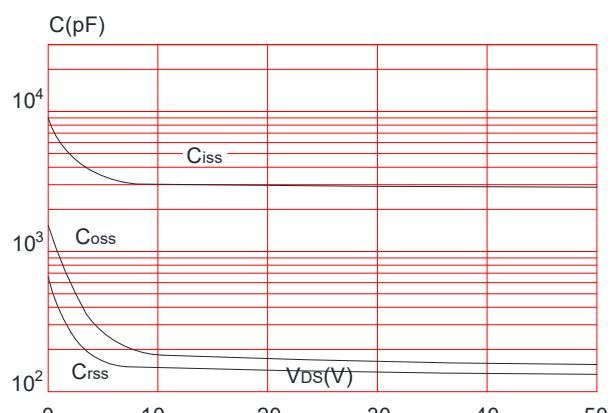


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

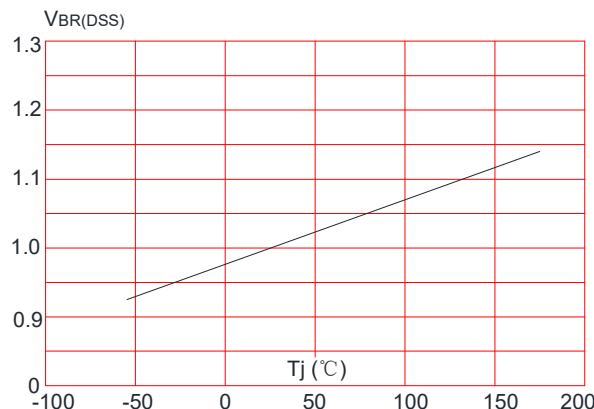


Figure 8: Normalized on Resistance vs. Junction Temperature

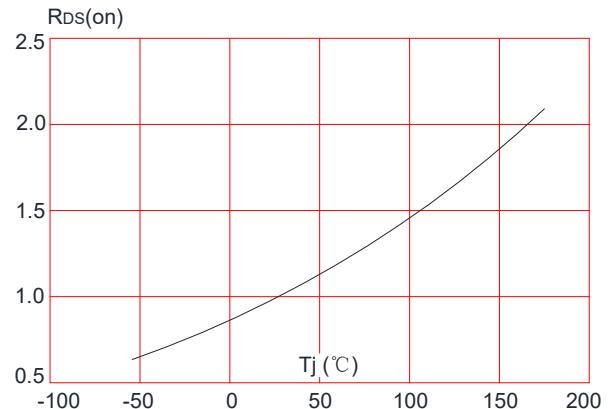


Figure 9: Maximum Safe Operating Area

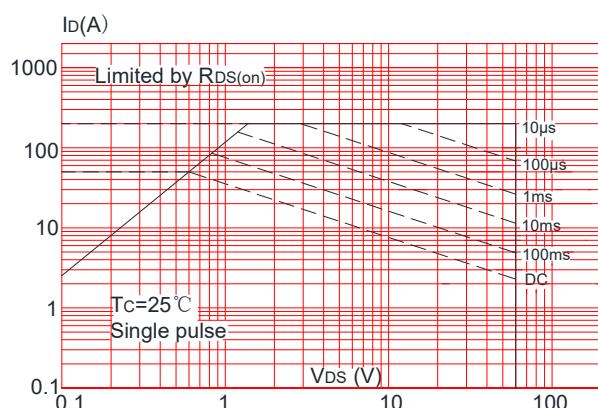


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

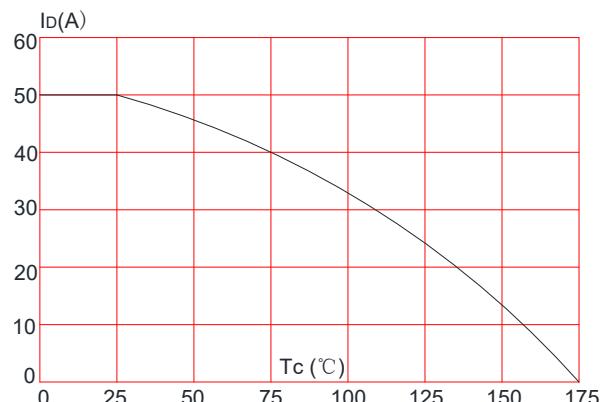
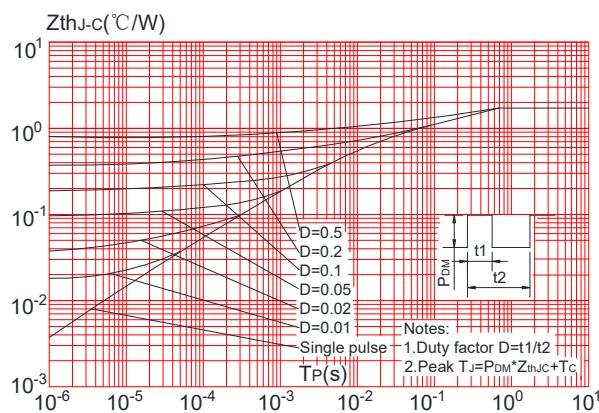
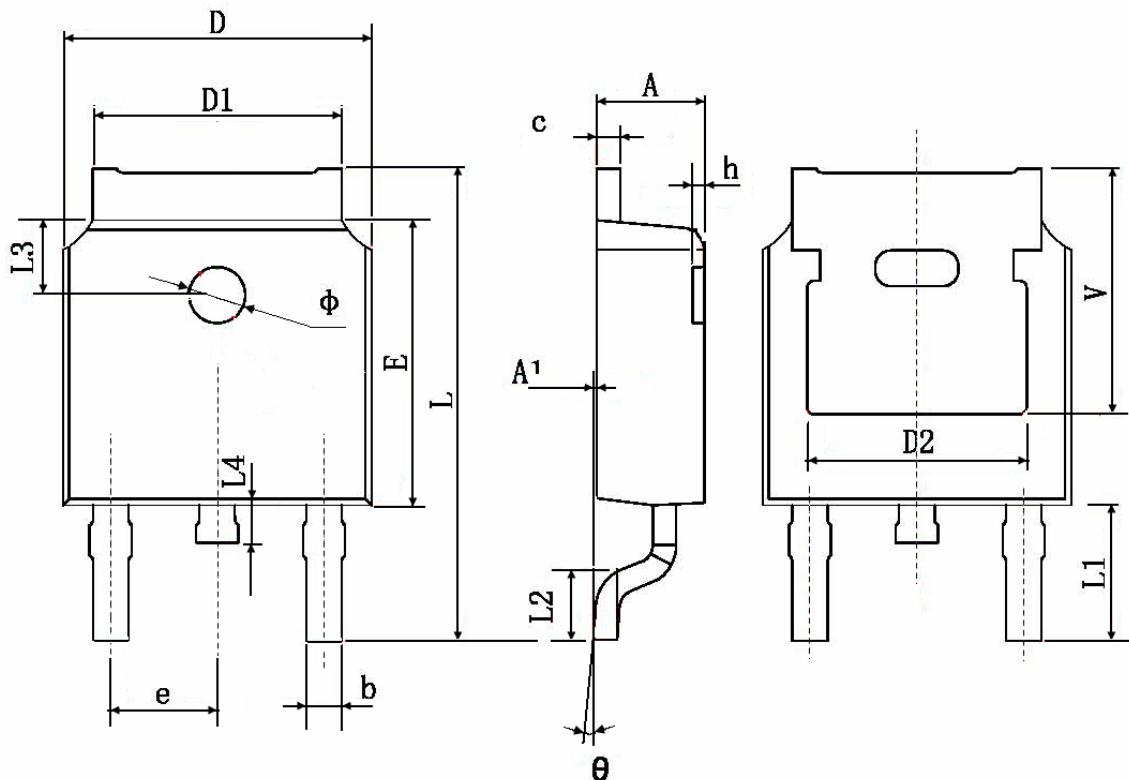


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Package Information: TO-252-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	